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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/091,766	03/05/2002	Mark Alan McClain	F1100	6836

7590 01/14/2005

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EXAMINER	
CHERY, MARDOCHEE	
ART UNIT	**PAPER NUMBER**
2188	

DATE MAILED: 01/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/091,766	MCCLAIN, MARK ALAN	
	Examiner	Art Unit	
	Mardochee Chery	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 March 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 March 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to Application No. 10/091766 filed on March 5, 2002.

Drawings

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: "system reset signal 61" on page 4, line 17. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claim 1,3-4,6-14, and 15-23, are rejected under 35 U.S.C. 102(e) as being anticipated by Gibson et al. (6,601,167).

As per claim 1, Gibson et al. discloses a non-volatile memory that has a sequential access style memory interface [*a computer system which includes a processor, a sequential access memory*; col.2, lines 22-24; *in response to initialization of the computer system controls the sequential access memory to read the first page of sequential memory containing a first portion of the boot program; the sequential memory can only deliver sequential words of memory*; col.2, lines 26-33].

As per claim 3, Gibson et al. discloses a method of initializing a computer system [*the boot loader includes a state machine, which in response to initialization of the computer system*; col.2, lines 25-26]; reading boot code stored in a non-volatile memory [*read the first page of sequential memory (Flash memory, EEPROM) containing a first portion of the boot program*; Fig.8; *Sequential Access Memory 32*; col.2, lines 27-29]; the first memory location in the non-volatile memory is read using at least one control signal that functions independently of the SDRAM style interface [*the boot program is configured to control the processor to transfer boot code from the sequential access memory to a volatile Random Memory (RAM) using move immediate*

instructions; col.14, lines 37-41; *the computer system controls the sequential access memory to read the first page of sequential memory containing a first portion of the boot program*; col.2, lines 26-29].

As per claim 4, Gibson et al. discloses subsequent memory locations are read by means of at least one control signal that functions independently of the SDRAM style interface and is received by sequential access logic incorporated in the non-volatile memory [*the computer system controls the sequential access memory to read the first page of sequential memory containing a first portion of the boot program*; col.2, lines 26-29].

As per claim 6, Gibson et al. discloses a method of configuring a SDRAM interface in a computer system [*initial program execution must occur in the non-volatile ROM at least until the sequential access memory has been set up for reading and programs in the sequential access memory can be transferred to volatile Random Access Memory (RAM)*; col.2, lines 2-6]; the computer system has a non-volatile memory with a SDRAM style interface [*the boot is configured to control the processor to transfer boot code from the sequential access memory to a volatile Random Memory (RAM)*; col.13, lines 32-35]; storing interface initialization code starting at the first location in the first accessed memory row of the non-volatile memory [*computer system includes a non-volatile Read Only Memory (ROM) which contains boot code instructions*; col.1, lines 17-19; *a sequential access memory having a boot program stored therein*; col.2, lines 23-24]; providing at least one control signal independent of the SDRAM style interface for incrementing the internal address of the non-volatile memory [*the boot loader includes a state machine, which in response to initialization of the computer system controls the sequential access memory to read the first page of sequential memory containing a first portion of the boot program*; col.2,

lines 25-29]; providing at least one control signal independent of the SDRAM style interface for performing a read operation from the first location in the first accessed memory row of the non-volatile memory [*the boot program is configured to control the processor to transfer boot code from the sequential access memory to a volatile Random Memory (RAM) using move immediate instructions*; col.14, lines 37-41; *the computer system controls the sequential access memory to read the first page of sequential memory containing a first portion of the boot program*; col.2, lines 26-29].

As per claim 10, Gibson et. al. discloses a computer system, non-volatile memory, and volatile memory, the non-volatile memory and volatile memory have a common interface [*initial program execution must occur in the non-volatile ROM at least until the sequential access memory has been set up for reading and programs in the sequential access memory can be transferred to volatile Random Access Memory (RAM)*; col.2, lines 2-6].

As per claim 20, Gibson et al. discloses, a computer system, a non-volatile memory having a SDRAM style interface [*the boot program is configured to control the processor to transfer boot code from the sequential access memory (Flash memory) to a volatile Random Memory (RAM)*; col.14, lines 37-41].

As per claim 7, Gibson et al. discloses the interface initialization code performs no branch operations [*the boot code stored in the flash device will not cause the micro-controller to branch or jump either forward or backward*; col.11, lines 20-22].

As per claims 8 and 9, the rationale in the rejection of claim 6 above is herein incorporated. Gibson et al. further discloses a final instruction for branching to the system initialization code in the random access memory [*the system is configured to jump to a predetermined memory address and begin executing the boot code upon initialization*; col.1, lines 24-27].

As per claim 11, applicant's attention is directed to the rejection of claim 10 supra.

As per claims 12-13, 18-19, and 22-23, applicant's attention is directed to the rejection of claim 6 above.

As per claim 14, Gibson et al. discloses the interface initialization code for initializing the interface includes no branch operations until the system is ready to provide random access to memory [*once the second portion of the boot code is copied to RAM, the first portion of the boot code executes a branch (jump) instruction*; col.2, lines 33-35].

As per claim 15, applicant's attention is directed to the rejection of claim 3 supra.

As per claim 16, Gibson et al. discloses a copy instruction is included after the interface initialization code, for copying boot code to a random access memory, and a branch instruction is included after the copy instruction for branching to the copied code

in the random access memory [*a boot code ROM in which an instruction or data at any address can be accessed; supports the branching behavior of most programs in which an instruction following a branch can be read*; col.1, lines 30-34; *initial program execution must occur in the non-volatile ROM at least until the sequential access memory has been set up for reading and programs in the sequential access memory can be transferred to volatile Random Access Memory (RAM) for execution*; col.2, lines 2-6].

As per claim 17, Gibson et al. discloses the interface initialization code is followed by a jump command to jump to a location in the non-volatile memory where the first instruction of at least part of the system boot code is stored *[the system is configured to jump to a predetermined memory address in the ROM and begin executing the boot code upon initialization of the system*; col.1, lines 24-27].

As per claim 21, Gibson et al. discloses the non-volatile memory is Flash memory [*the system code is stored in UltraNAND flash memory*; col.6, lines 47-48; *this memory is a flash ROM device based on NAND architecture*; col.1, lines 49-50].

5. Claim 5 is rejected under 35 U.S.C. 102(e) as being anticipated by Wisor (6,823,435).

As per claim 5, Wisor discloses a method of reducing control and address lines in a computer system having non-volatile memory and SDRAM [*the non-volatile memory cells*

are accessed using address signals driven upon the address lines of memory bus 20; col.4, lines 58-60].

6. Claim 2 is rejected under 35 U.S.C. 102(e) as being anticipated by Zarrin et al. (6,128,731).

As per claim 2, Zarrin et al. discloses a computer system that includes non-volatile memory and SDRAM, the non-volatile memory shares a common interface with SDRAM [*the computer system includes one or more processors coupled to a volatile memory (e.g., SDRAM) and a non-volatile memory (e.g., flash memory) via one or more buses*; col.4, lines 19-22].

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Gibson et al.	6,601,167
Zarrin et al.	6,128,731
Wisor	6,823,435

8. When responding to the office action, Applicant is advised to clearly point out the patentable novelty that he or she thinks the claims present in view of the state of the art disclosed by references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 C.F.R. 1.111(c).

9. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mardochee Chery whose telephone number is (571)272-4246. The examiner can normally be reached on 8:30A-5:00P.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Manonama Padmanabhan can be reached on (571)272-4210. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

January 6, 2005

M C

Mardochee Chery
Examiner
AU: 2188

January 7, 2005

Pierre M. Vital

Pierre M.Vital
Primary Examiner
AU2188